What is claimed is:

1. A semiconductor device comprising:

a semiconductor chip having a first main surface on which a plurality of electrode pads are provided, a second main surface which opposes said first main surface, and a plurality of side surfaces positioned between said first main surface and said second main surface;

an extension portion formed in contact with said side surfaces of said semiconductor chip so as to surround said semiconductor chip;

an insulating film formed on a surface of said extension portion and said first main surface such that a part of each of said electrode pads is exposed;

a plurality of wiring patterns formed on said insulating film so as to be electrically connected to said electrode pads , respectively and extended from said electrode pads to the surface of said extension portion;

a sealing portion formed on said wiring patterns and said insulating film such that a part of said wiring patterns is exposed; and

a plurality of external terminals provided over said wiring patterns in a region including the upper side of said extension portion.

2. The semiconductor device according to claim 1, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals,

wherein said sealing portion is formed such that the

top surface of said electrode posts is exposed.

3. The semiconductor device according to claim 1, wherein said electrode posts are formed from a conductive material.

4. The semiconductor device according to claim 3, wherein a thin oxidation layer is formed on a surface of said electrode posts.

5. The semiconductor device according to claim 1, wherein said external terminals are formed as solder balls.

6. The semiconductor device according to claim 1, wherein said external terminals are lands.

7. The semiconductor device according to claim 1, wherein a portion of said wiring patterns on a boundary and vicinity of a boundary between said semiconductor chip and said extension portion is formed more thickly than other portions of said wiring patterns.

8. The semiconductor device according to claim 1, wherein said extension portion is formed from a material having a greater molding shrinkage than the molding shrinkage of said sealing portion.

9. The semiconductor device according to claim 8, wherein said extension portion is formed from a liquid resin having a linear expansion coefficient in a lower temperature range than glass transition temperature of less than 1.5×10^{-5}/°C and a modulus of elasticity within a range of 7.8 to 22 GPa.

10. A semiconductor device comprising:

a semiconductor chip having a first main surface on

which a plurality of electrode pads is provided, a second main surface which opposes said first main surface, and a plurality of side surfaces positioned between said first main surface and said second main surface;

an extension portion formed in contact with said side surfaces of said semiconductor chip so as to surround said semiconductor chip;

a passive element comprising connection terminals and provided on said extension portion;

an insulating film formed on a surface of said extension portion and said first main surface such that a part of each of said electrode pads and a part of said connection terminals are exposed;

a plurality of wiring patterns electrically connected to said electrode pads, respectively and extended from said electrode pads to the surface of said extension portion;

a sealing portion formed on said wiring patterns and said insulating film such that a part of said wiring patterns is exposed; and

a plurality of external terminals provided over said wiring patterns in a region including the upper side of said extension portion.

11. The semiconductor device according to claim 10, wherein a portion of said wiring patterns on a boundary and vicinity thereof between said semiconductor chip and said extension portion is formed more thickly than other portions of said wiring patterns.

12. The semiconductor device according to claim 10,

wherein said passive element provided on said extension portion comprises a plurality of connection terminals, one of said connection terminals being connected to said electrode pads and the other connection terminal being connected to said external terminals.

13. The semiconductor device according to claim 10, wherein said passive element provided on said extension portion comprises a plurality of connection terminals, one of said connection terminals being connected to a specific external terminal and the other connection terminal being connected to a different external terminal.

14. The semiconductor device according to claim 10, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals,

wherein said sealing portion is formed such that the top surface of said electrode posts is exposed.

15. The semiconductor device according to claim 10, wherein said electrode posts are formed from a conductive material.

16. The semiconductor device according to claim 10, wherein a thin oxidation layer is formed on a surface of said electrode posts.

17. The semiconductor device according to claim 10, wherein said external terminals are solder balls.

18. The semiconductor device according to claim 10, wherein said external terminals are lands.

19. The semiconductor device according to claim 10,

wherein said extension portion is formed from a material having a greater molding shrinkage than the molding shrinkage of said sealing portion.

20. The semiconductor device according to claim 19, wherein said extension portion is formed from a liquid resin having a linear expansion coefficient in a lower temperature range than glass transition temperature of less than 1.5×10^{-5}/°C and a modulus of elasticity within a range of 7.8 to 22 GPa.